twareLAB

# 4CH S2E Module

Datasheet Ver1.2

twareLAB

# Contents

# 1 INTRODUCTION

## 1.1 KEY FEATURES

- 4 Port Serial-to-Ethernet
- Support DHCP IP Acquisition
- Support DNS Query
- Support NTP Time Query
- Support Time Zone Setting
- TCP/UDP Data Communication
- Ethernet Data Packing Option
- Support Up to 3Mbps UART Baud Rate

## 1.2 PRODUCT SPECIFICATIONS

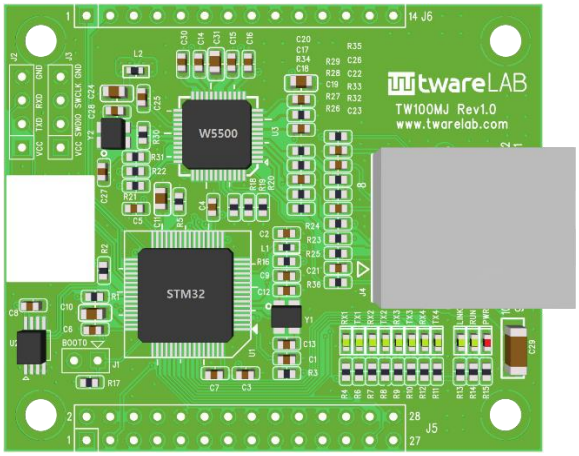
| | Specification |
|---|---|
| MCU | STM32F405RGT6 (RAM: 192Kbyte, FLASH: 1Mbyte) |
| LAN | W5500 (10/100Mbps Ethernet) |
| UART | 4 Port (3.3V TTL Level) |
| Console Port | Supported |
| Dimension | TW100MJ: 48.26(W)x61.4(H)x22(D), TW100XR: 48.26(W)x58.00(H)x15(D) |
| Connector | 2.54mm Pitch Pin Header. J5: 2x14, J6: 1x14 |
| Input Power | DC 3.3V |
| Power Dissipation | Typical: 100mA, Peak: 150mA |
| Temperature | Operation: 0℃ ~ +70℃, Storage: -40℃ ~ +85℃ |
| Humidity | 10 ~ 80% |

# 2 HARDWARE SPECIFICATION

## 2.1 DESCRIPTION

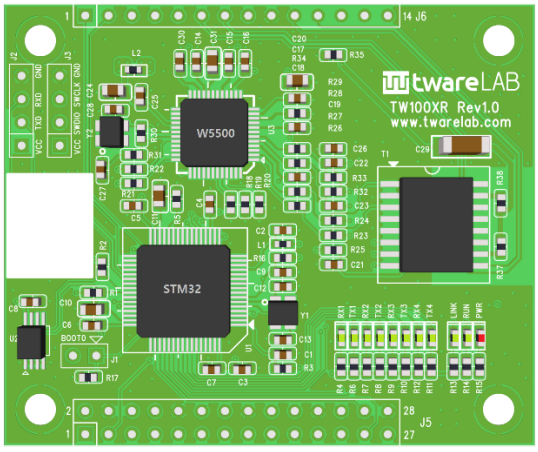
### 2.1.1 TW100MJ

- RJ45 embedded (Ethernet Transformer inside)
- 2.54 pitch pin header interface (42 pins)

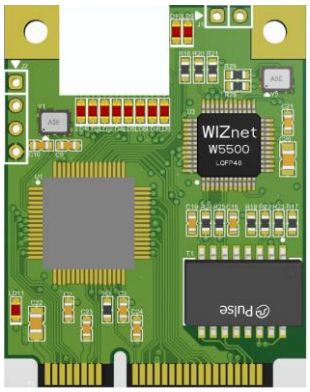



### 2.1.2 TW100XR

- Ethernet Transformer embedded
  - RJ45 is needed on the customer board
- 2.54 pitch pin header interface (42 pins)



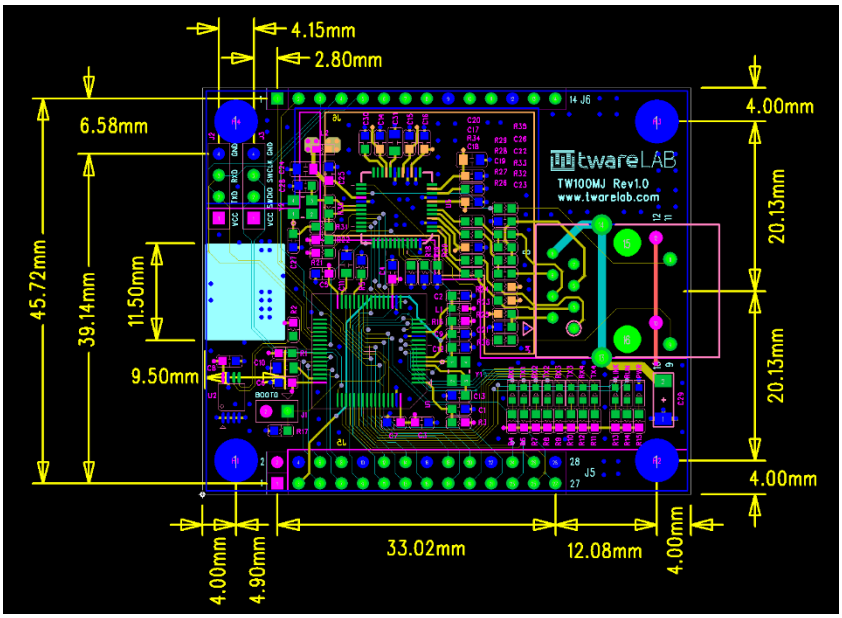
### 2.1.3 TW100PC



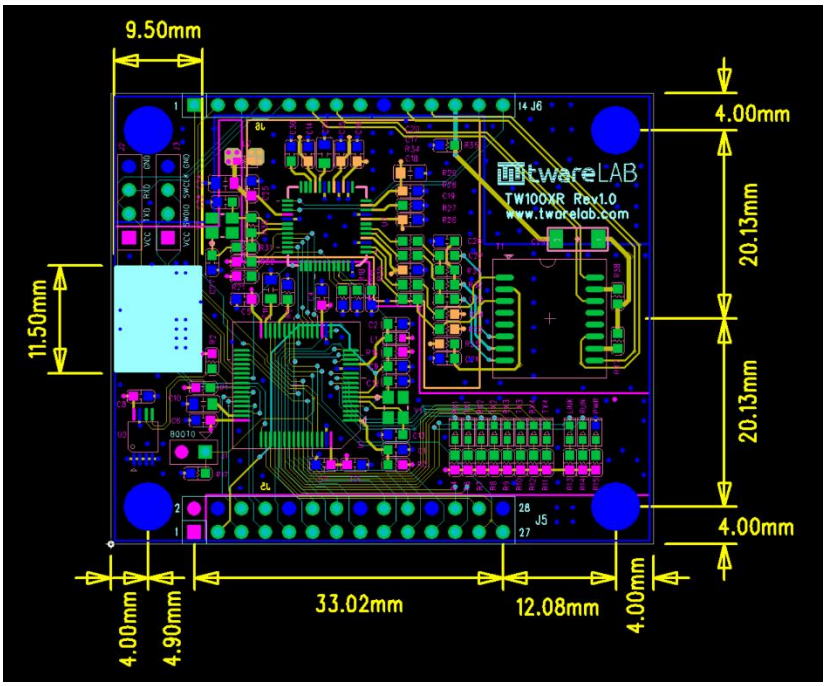

- Ethernet Transformer embedded
  - RJ45 is needed on the customer board
- miniPCI interface (52 pins)

## 2.2 DIMENSION

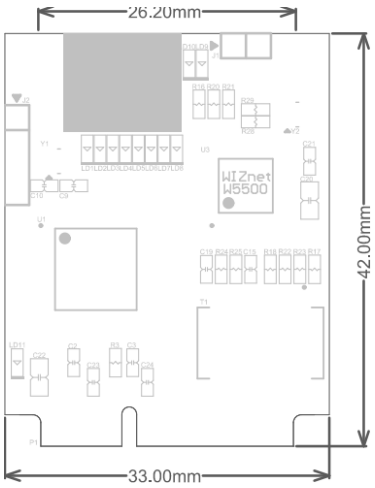
### 2.2.1 TW100MJ



### 2.2.2 TW100XR



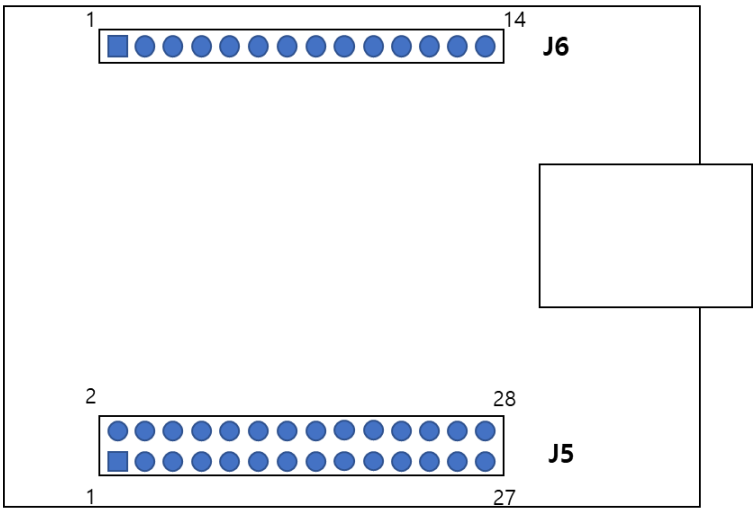

### 2.2.3 TW100PC



## 2.3 PIN MAP

### 2.3.1 TW100MJ / TW100XR

#### *2.3.1.1 Header Pin Layout*




#### *2.3.1.2 J5 Connector*

| Pins | Signal | I/O | Description |
|---|---|---|---|
| 1 | VCC_3.3 | S | Power 3.3V |
| 2 | VCC_3.3 | S | Power 3.3V |
| 3 | /RESET | I | Board Rest, Active Low |
| 4 | GND | S | Ground |
| 5 | UART1_RX | I | 3.3V TTL Level. |
| 6 | UART1_CTS | I | 3.3V TTL Level |
| 7 | UART1_TX | O | 3.3V TTL Level |
| 8 | UART1_RTS | O | 3.3V TTL Level |
| 9 | STATUS_1 | O | 1: TCP Disconnected, 0: TCP Connected |
| 10 | GND | S | Ground |
| 11 | UART2_RX | I | 3.3V TTL Level. |
| 12 | UART2_CTS | I | 3.3V TTL Level |
| 13 | UART2_TX | O | 3.3V TTL Level |
| 14 | UART2_RTS | O | 3.3V TTL Level |
| 15 | STATUS_2 | O | 1: TCP Disconnected, 0: TCP Connected |
| 16 | GND | S | Ground |
| 17 | UART3_RX | I | 3.3V TTL Level. |
| 18 | UART3_CTS | I | 3.3V TTL Level |
| 19 | UART3_TX | O | 3.3V TTL Level |

| | | | |
|---|---|---|---|
| 20 | UART3_RTS | O | 3.3V TTL Level |
| 21 | STATUS_3 | O | 1: TCP Disconnected, 0: TCP Connected |
| 22 | GND | S | Ground |
| 23 | UART4_RX | I | 3.3V TTL Level. |
| 24 | UART4_CTS | I | 3.3V TTL Level |
| 25 | UART4_TX | O | 3.3V TTL Level |
| 26 | UART4_RTS | O | 3.3V TTL Level |
| 27 | STATUS_4 | O | 1: TCP Disconnected, 0: TCP Connected |
| 28 | GND | S | Ground |

#### *2.3.1.3 J6 Connector*

| Pins | Signal | I/O | Description |
|---|---|---|---|
| 1 | SW_INPUT | I | SW Input for software reset. Internal Pull-Up. Active Low. |
| 2 | HW_TRIGGER | I | AT Command Mode Activate. Active Low. Internal Pull-Up |
| 3 | Console_TX | O | |
| 4 | Console_RX | I | |
| 5 | BOOT | I | Active High. Pin for STM32 Boot Mode |
| 6 | MDI_TXM | O | Differential Signal to RJ45. Available for only TW100XR |
| 7 | MDI_TXP | O | Differential Signal to RJ45. Available for only TW100XR |
| 8 | NC | | |
| 9 | GND | S | |
| 10 | MDI_RXM | I | Differential Signal to RJ45. Available for only TW100XR |
| 11 | MDI_RXP | I | Differential Signal to RJ45. Available for only TW100XR |
| 12 | AGND | S | Analog Ground |
| 13 | /LINK_LED | O | Active Low. LINK LED indicator. Available for only TW100XR |
| 14 | /ACT_LED | O | Active Low. ACT LED indicator. Available for only TW100XR |

### 2.3.2 TW100PC

#### *2.3.2.1 miniPCI Layout*


Front – odd number, 26pin

Back – even number, 26pin

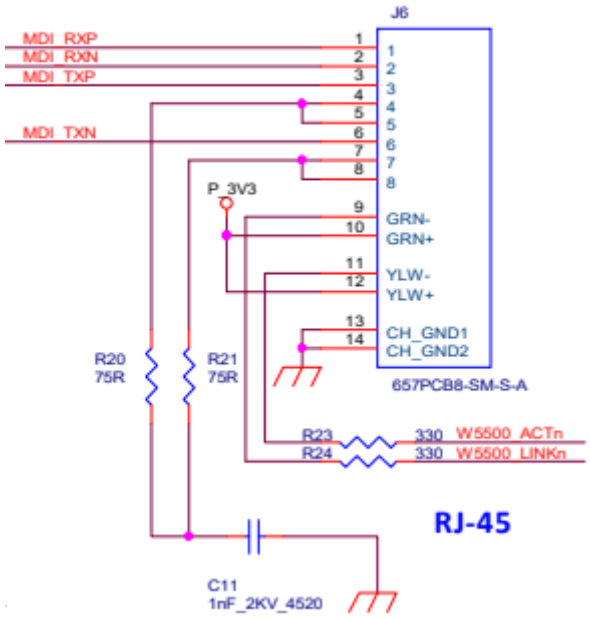
#### *2.3.2.2 miniPCI Connector*

| Pins | Signal | I/O | Description |
|---|---|---|---|
| 1 | VCC_3.3 | S | Power 3.3V |
| 2 | GND | S | Ground |
| 3 | NC | | |
| 4 | NC | | |
| 5 | NC | | |
| 6 | NRST | I | Board Rest, Active Low |
| 7 | UART2_CTS | I | 3.3V TTL Level |
| 8 | UART2_RTS | O | 3.3V TTL Level |
| 9 | UART2_TX | O | 3.3V TTL Level. |
| 10 | UART2_RX | I | 3.3V TTL Level |
| 11 | VCC_3.3 | S | Power 3.3V |
| 12 | GND | S | Ground |
| 13 | STATUS_1 | O | 1: TCP Disconnected, 0: TCP Connected |
| 14 | STATUS_2 | O | 1: TCP Disconnected, 0: TCP Connected |
| 15 | STATUS_3 | O | 1: TCP Disconnected, 0: TCP Connected |
| 16 | STATUS_4 | S | 1: TCP Disconnected, 0: TCP Connected |
| 17 | UART3_TX | O | 3.3V TTL Level. |
| 18 | UART3_RX | I | 3.3V TTL Level |
| 19 | NC | | |
| 20 | UART3_CTS | I | 3.3V TTL Level. |
| 21 | UART3_RTS | O | 3.3V TTL Level |
| 22 | SW_Input | I | SW Input for software reset. Internal Pull-Up. Active Low. |
| 23 | VCC_3.3 | S | Power 3.3V |
| 24 | GND | S | Ground |
| 25 | Console_TX | O | 3.3V TTL Level |
| 26 | Console_RX | O | 3.3V TTL Level |

| | | | |
|---|---|---|---|
| 27 | NC | | |
| 28 | NC | | |
| 29 | UART1_TX | O | 3.3V TTL Level. |
| 30 | UART1_RX | I | 3.3V TTL Level |
| 31 | UART1_CTS | I | 3.3V TTL Level. |
| 32 | UART1_RTS | O | 3.3V TTL Level |
| 33 | NC | | |
| 34 | NC | | |
| 35 | UART4_RTS | O | 3.3V TTL Level. |
| 36 | UART4_TX | O | 3.3V TTL Level |
| 37 | UART4_RX | I | 3.3V TTL Level. |
| 38 | UART4_CTS | I | 3.3V TTL Level |
| 39 | HW_TRIGGER | I | AT Command Mode Activate. Active Low. Internal Pull-Up |
| 40 | NC | | |
| 41 | NC | | |
| 42 | NC | | |
| 43 | VCC_3.3 | S | Power 3.3V |
| 44 | GND | S | Ground |
| 45 | /LINK_LED | | Active Low. LINK LED indicator |
| 46 | /ACT_LED | | Active Low. ACT LED indicator |
| 47 | MDI_RXN | | Differential Signal to RJ45 |
| 48 | MDI_TXN | | Differential Signal to RJ45 |
| 49 | MDI_RXP | | Differential Signal to RJ45 |
| 50 | MDI_TXP | | Differential Signal to RJ45 |
| 51 | NC | | |
| 52 | AGND | | |

## 2.4 REFERENCE SCHEMATIC

This is only for TW100XR and TW100PC.



# 3 HISTORY

| Date | Description |
|---|---|
| 2022-11-02 | V1.0 First Released |
| 2023-01-27 | V1.1 Add 2.5 Reference Schematic |
| 2023-11-25 | V1.2 STATUS pins, SW_Input pin, Boot pin description updated |